CLAIMS

1. A method for displaying image data on an RGB panel and a parallel panel simultaneously, comprising the operations of:

setting an RGB panel to accept image data from a set of data lines;

transmitting RGB image data to the RGB panel using the set of data lines, wherein the RGB image data is transmitted at a rate based on an RGB clock;

setting a parallel panel to accept image data from the set of data lines; and

transmitting parallel image data to the parallel panel using the set of data lines, wherein the parallel image data is transmitted at a rate based on a parallel clock.

2. The method of claim 1, wherein the RGB panel is set to decline image data from a set of data lines when the parallel panel is set to accept image data from the set of data lines, and wherein the parallel panel is set to decline image data from a set of data lines when the RGB panel is set to accept image data from the set of data lines.

3. The method of claim 2, wherein the RGB panel is set to accept image data from the set of data lines when an RGB select signal is high.

4. The method of claim 3, wherein the RGB select signal is an RGB resynchronization signal.

5. The method of claim 1, further comprising:

synchronizing image data transfer to the RGB panel and the parallel panel.

6. The method of claim 5, wherein the method operation of synchronizing image data transfer to the RGB panel and the parallel panel includes,

establishing a shared data clock;

determining if the RGB panel active;

if the RGB panel is active, the method includes,

setting a rate of the shared data clock to correspond to a rate of the RGB clock and;

if the RGB panel is inactive, the method includes,

setting a rate of the shared data clock to correspond to a rate of the parallel clock.

7. A graphics controller, comprising:

circuitry for updating multiple display panels over a shared set of data lines associated with the multiple display panels, the circuitry for updating multiple display panels includes,

circuitry for generating control signals over control lines dedicated to each of the multiple display panels;

a memory region configured to store image data for display on the multiple display panels; and

circuitry configured to select image data associated with one of the multiple display panels for display during an inactive period associated with an other one of the multiple display panels.

8. The graphics controller of claim 7, wherein the multiple panels include a single RGB panel and a single parallel panel.

9. The graphics controller of claim 7, further comprising:

circuitry configured to synchronize image data transfer according to a clock associated with an active one of the multiple display panels.

10. The graphics controller of claim 7, wherein the circuitry configured to select image data associated with one of the multiple display panels for display during an inactive period associated with an other one of the multiple display panels includes,

a multiplexer configured to select data for one of a parallel panel and a RGB panel.

11. The graphics controller of claim 7, wherein the shared set of data lines includes eighteen data lines.

12. The graphics controller of claim 7, wherein the memory region provides all memory support for each of the multiple display panels.

13. The graphics controller of claim 9, wherein the circuitry configured to synchronize image data transfer according to a clock associated with an active one of the multiple display panels is further configured to select image data from the memory region according to the circuitry for generating the control signals.

14. A device, comprising:

multiple display panels;

a graphics controller configured to drive the multiple display panels over a shared set of data lines, the graphics controller including circuitry configured to select image data associated with one of the multiple display panels for display during an inactive period associated with an other one of the multiple display panels; and

a shared clock configured to synchronize image data transfer based upon a clock rate associated with the active period.

15. The device of claim 14, wherein the multiple display panels includes a RGB panel and a parallel panel.

16. The device of claim 14, wherein each of the multiple display panels is associated with a different clock rate.

17. The device of claim 14, where a number of shared data lines is eighteen.

18. The device of claim 14, wherein the device is a cellular phone having a primary panel and a secondary panel.

19. The device of claim 14, wherein the graphics controller further includes,

a memory shared by each of the multiple display panels.

20. The device of claim 14, wherein the circuitry configured to select image data includes control logic configured to generate control signals associated with the one of the multiple display panels.